

# 74HC02; 74HCT02

## Quad 2-input NOR gate

Rev. 03 — 18 September 2008

Product data sheet

## 1. General description

The 74HC02; 74HCT02 are high-speed Si-gate CMOS devices that comply with JEDEC standard no. 7A. They are pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC02; 74HCT02 provides a quad 2-input NOR function.

## 2. Features

- Input levels:
  - ◆ For 74HC02: CMOS level
  - ◆ For 74HCT02: TTL level
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74HC02N	-40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)		SOT27-1
74HCT02N					
74HC02D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm		SOT108-1
74HCT02D					
74HC02DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm		SOT337-1
74HCT02DB					
74HC02PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm		SOT402-1
74HCT02PW					
74HC02BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm		SOT762-1
74HCT02BQ					

## 4. Functional diagram

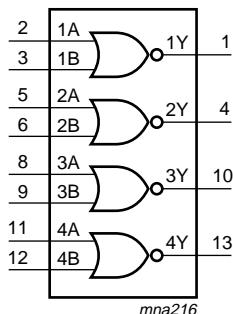


Fig 1. Logic symbol

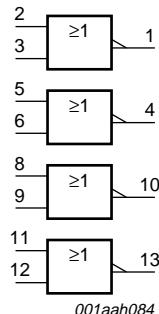


Fig 2. IEC logic symbol

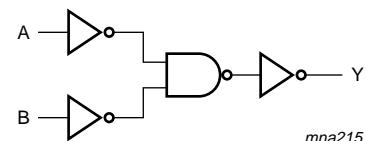


Fig 3. Logic diagram (one gate)

## 5. Pinning information

### 5.1 Pinning

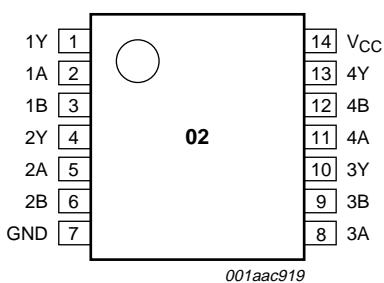
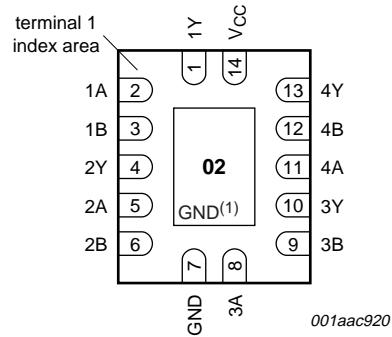


Fig 4. Pin configuration DIP14, SO14 and (T)SSOP14



Transparent top view

- (1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 5. Pin configuration DHVQFN14

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y to 4Y	1, 4, 10, 13	data output
1A to 4A	2, 5, 8, 11	data input
1B to 4B	3, 6, 9, 12	data input
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3. Function table<sup>[1]</sup>**

Input	nB	Output
nA		nY
L	L	H
X	H	L
H	X	L

[1] H = HIGH voltage level;

L = LOW voltage level;

X = don't care.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	<sup>[1]</sup> -	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	<sup>[1]</sup> -	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation		<sup>[2]</sup>		
	DIP14 package		-	750	mW
	SO14, (T)SSOP14 and DHVQFN14 packages		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP14 package: P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.

For SO14 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

For (T)SSOP14 packages: P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN14 packages: P<sub>tot</sub> derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC02			74HCT02			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	-40	-	+125	°C

**Table 5. Recommended operating conditions ...continued**

Voltages are referenced to GND (ground = 0 V) ...continued

Symbol	Parameter	Conditions	74HC02			74HCT02			Unit
			Min	Typ	Max	Min	Typ	Max	
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0 \text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5 \text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC02</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0 \text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5 \text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0 \text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0 \text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5 \text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0 \text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -20 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20 \mu\text{A}; V_{CC} = 6.0 \text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 20 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu\text{A}; V_{CC} = 6.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	20	-	40	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT02</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = −20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = −4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	2.0	-	20	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> − 2.1 V; I <sub>O</sub> = 0 A; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V	-	150	540	-	675	-	735	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**GND = 0 V; C<sub>L</sub> = 50 pF; for load circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	
<b>74HC02</b>								
t <sub>pd</sub>	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a>	[1]					
		V <sub>CC</sub> = 2.0 V	-	25	90	115	135	ns
		V <sub>CC</sub> = 4.5 V	-	9	18	23	27	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	7	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	7	15	20	23	ns
t <sub>t</sub>	transition time	see <a href="#">Figure 6</a>	[2]					
		V <sub>CC</sub> = 2.0 V	-	19	75	95	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	19	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	16	19	ns
C <sub>PD</sub>	power dissipation capacitance	per package; V <sub>I</sub> = GND to V <sub>CC</sub>	[3]	-	22	-	-	pF

**Table 7. Dynamic characteristics***GND = 0 V;  $C_L = 50 \text{ pF}$ ; for load circuit see [Figure 7](#).*

Symbol	Parameter	Conditions	25 °C			−40 °C to +125 °C		Unit	
			Min	Typ	Max	Max (85 °C)	Max (125 °C)		
<b>74HCT02</b>									
$t_{pd}$	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a>	[1]						
		$V_{CC} = 4.5 \text{ V}$	-	11	19	24	29	ns	
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	9	-	-	-	ns	
$t_t$	transition time	$V_{CC} = 4.5 \text{ V}$ ; see <a href="#">Figure 6</a>	[2]	-	7	15	19	22	ns
$C_{PD}$	power dissipation	per package;	[3]	-	24	-	-	-	pF
	capacitance	$V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$							

[1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

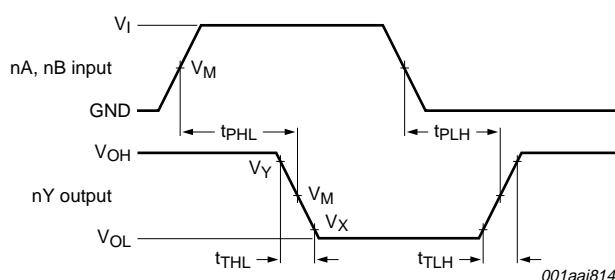
$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 $f_i$  = input frequency in MHz; $f_o$  = output frequency in MHz; $C_L$  = output load capacitance in pF; $V_{CC}$  = supply voltage in V;

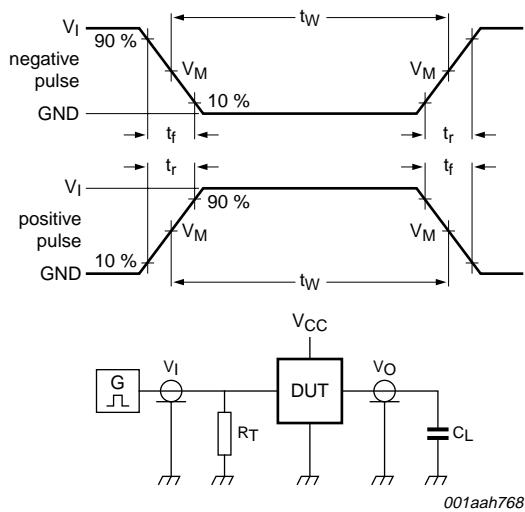
N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## 11. Waveforms

Measurement points are given in [Table 9](#). $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.**Fig 6. Input to output propagation delays****Table 8. Measurement points**

Type	Input		Output		
	$V_M$		$V_M$	$V_X$	$V_Y$
74HC02	0.5 $V_{CC}$		0.5 $V_{CC}$	0.1 $V_{CC}$	0.9 $V_{CC}$
74HCT02	1.3 V		1.3 V	0.1 $V_{CC}$	0.9 $V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

**Fig 7. Load circuitry for measuring switching times**

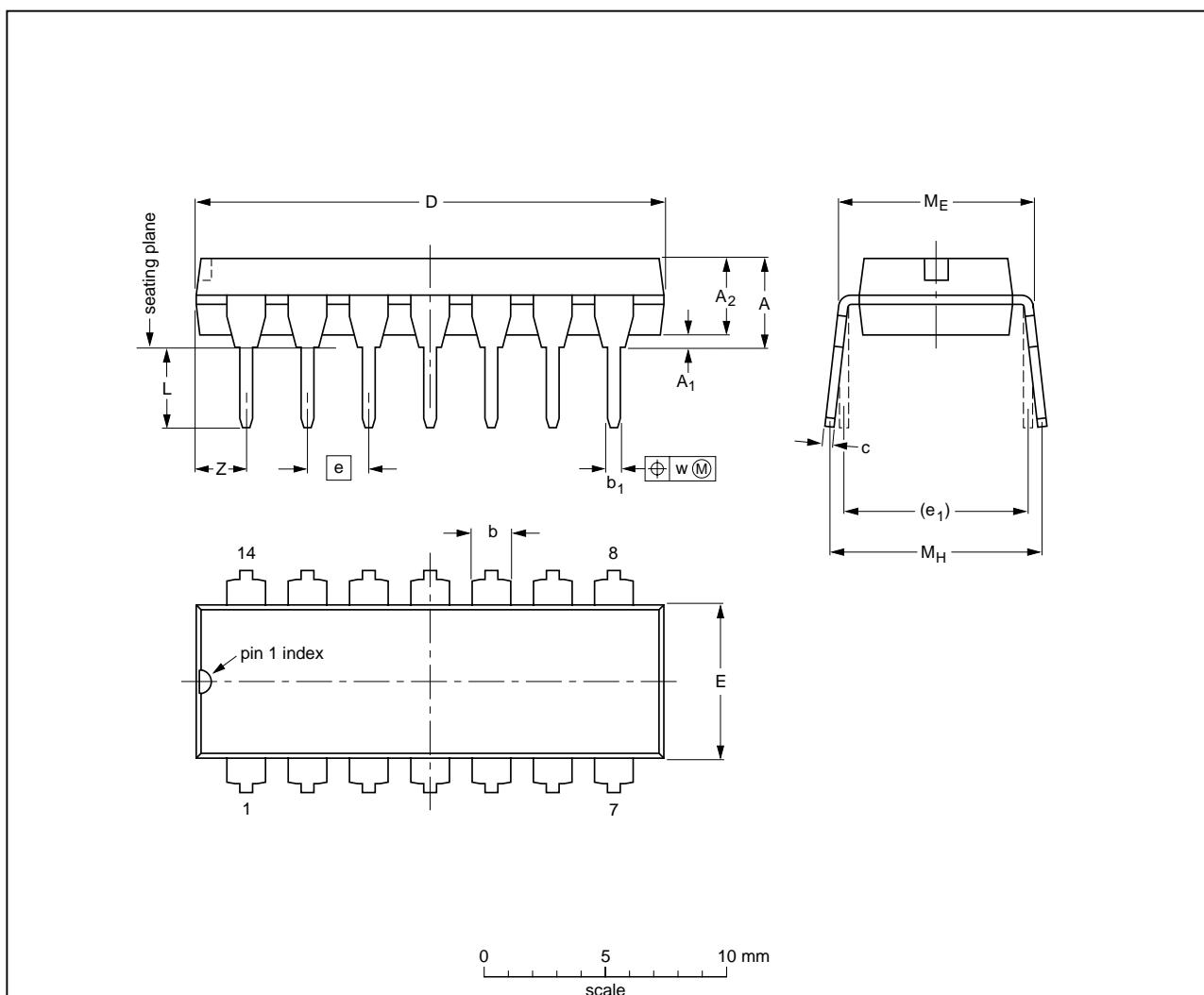
**Table 9. Test data**

Type	Input		Load	Test
	$V_I$	$t_r, t_f$		
74HC02	$V_{CC}$	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74HCT02	3.0 V	6.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

## 12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			99-12-27 03-02-13

**Fig 8. Package outline SOT27-1 (DIP14)**

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

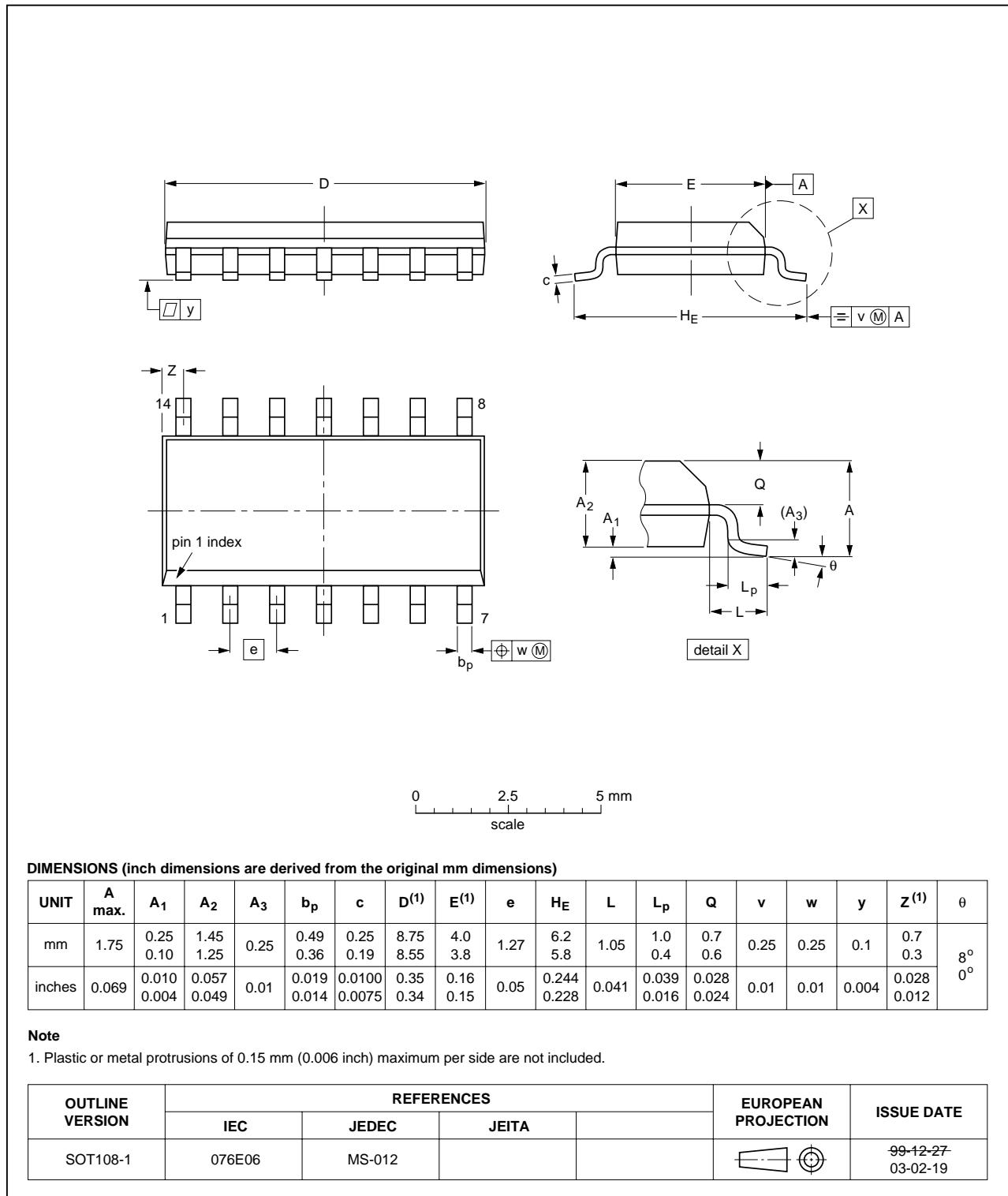


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

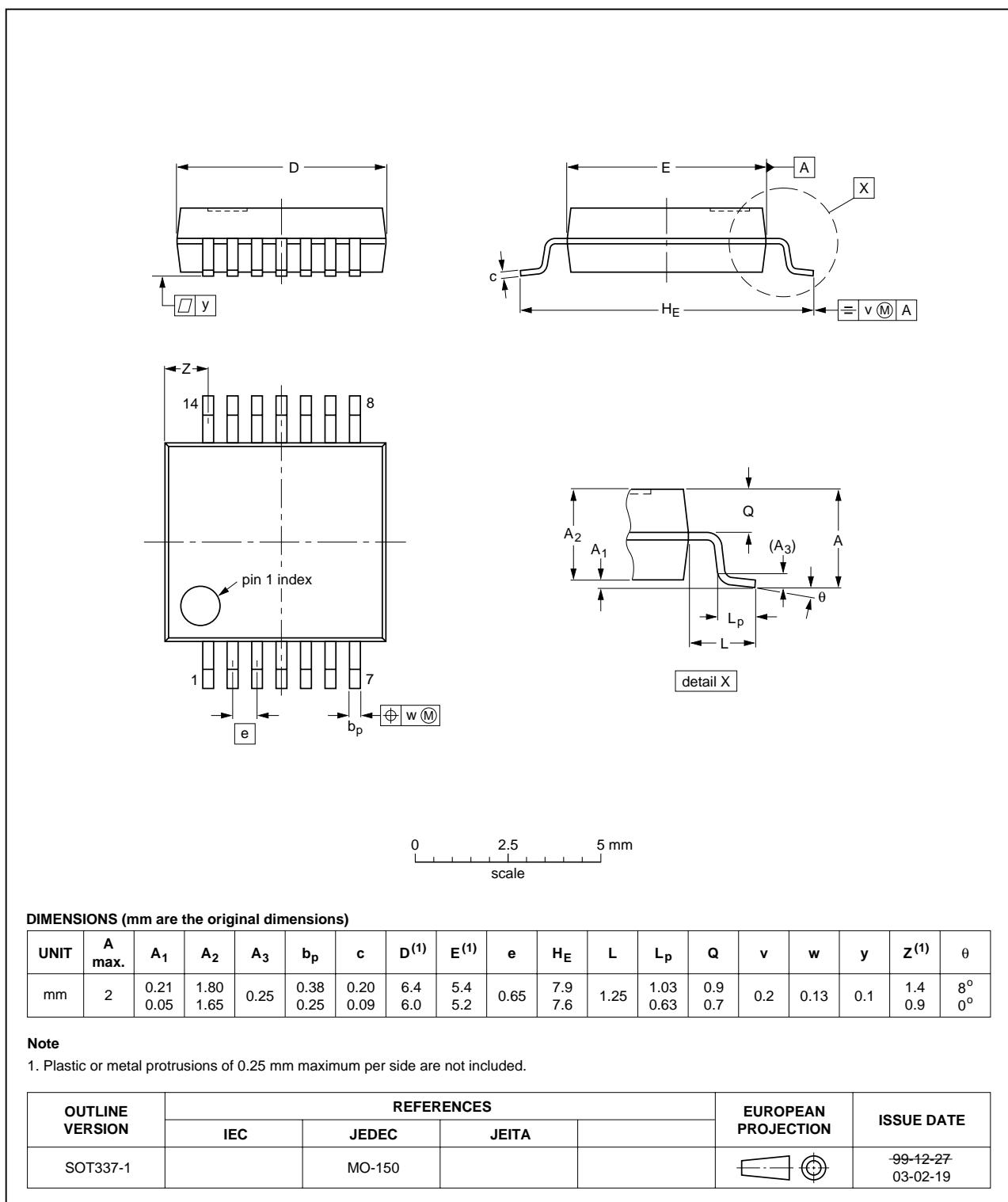


Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

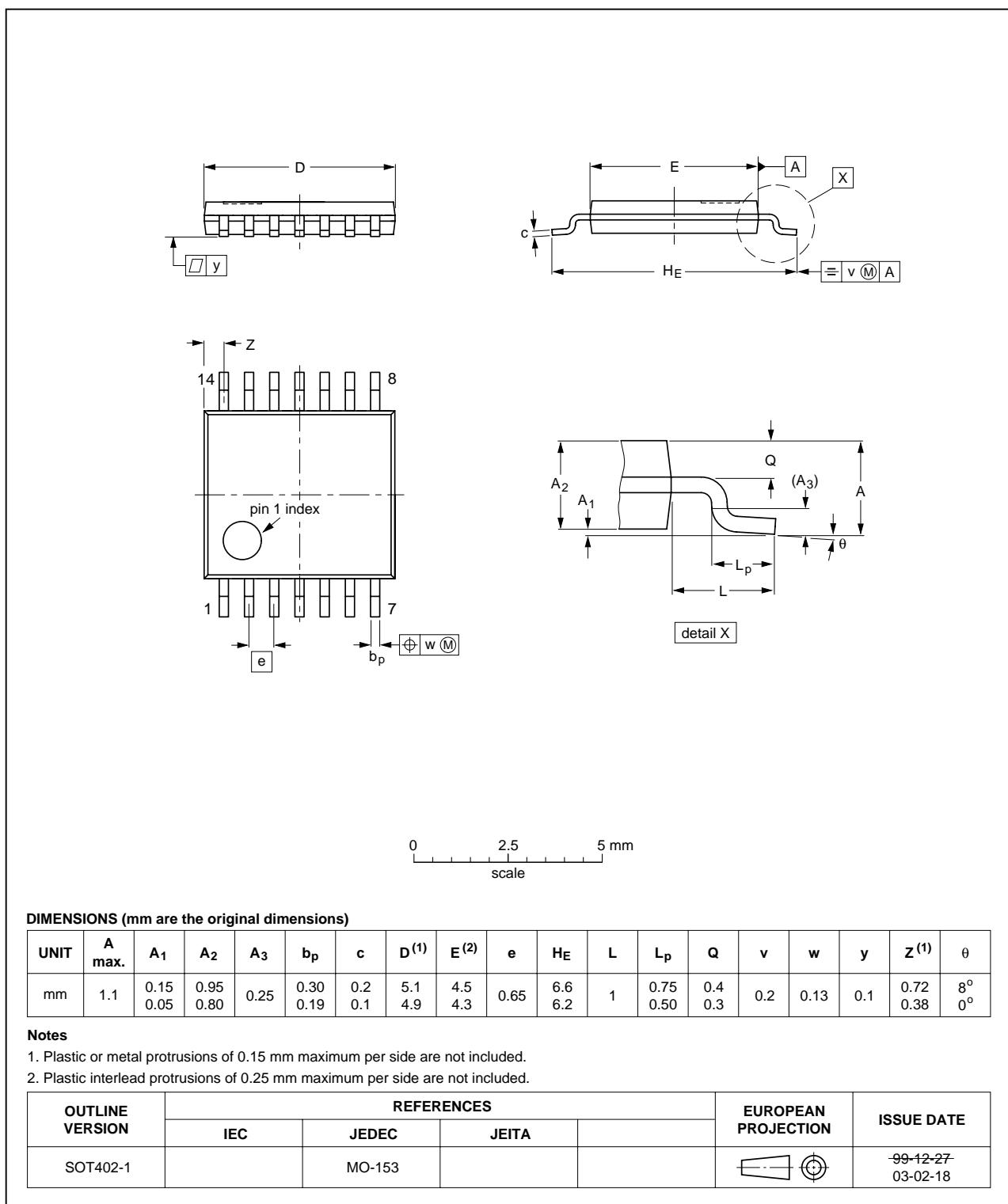


Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
14 terminals; body 2.5 x 3 x 0.85 mm  
SOT762-1

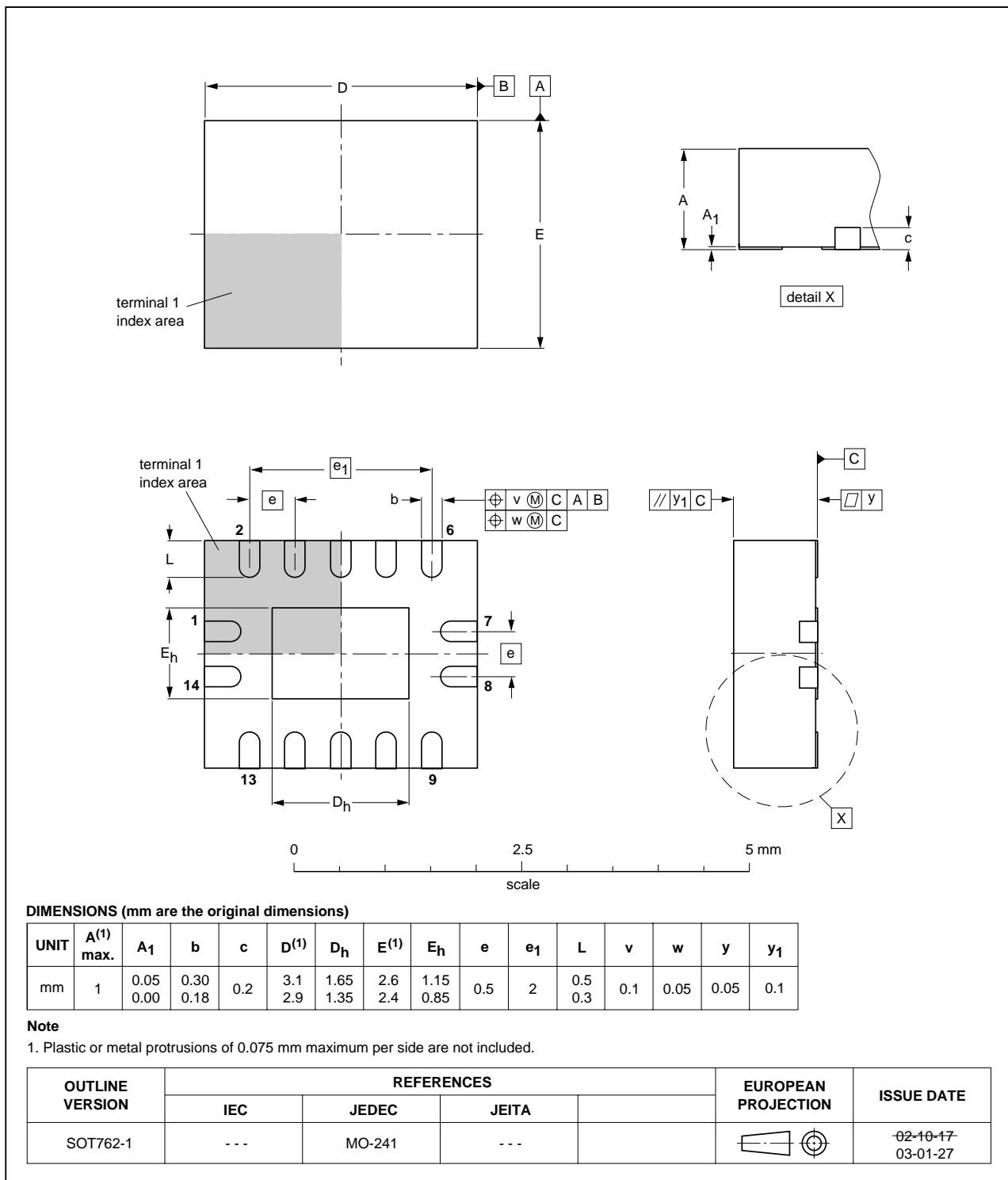


Fig 12. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT02_3	20080918	Product data sheet	-	74HC_HCT02_CNV_2
Modifications:		<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Added type numbers 74HC02BQ and 74HCT02BQ (DHVQFN14 package)</li> </ul>		
74HC_HCT02_CNV_2	19970827	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 15.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfuction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 17. Contents

<b>1</b>	<b>General description</b>	<b>1</b>
<b>2</b>	<b>Features</b>	<b>1</b>
<b>3</b>	<b>Ordering information</b>	<b>1</b>
<b>4</b>	<b>Functional diagram</b>	<b>2</b>
<b>5</b>	<b>Pinning information</b>	<b>2</b>
5.1	Pinning	2
5.2	Pin description	2
<b>6</b>	<b>Functional description</b>	<b>3</b>
<b>7</b>	<b>Limiting values</b>	<b>3</b>
<b>8</b>	<b>Recommended operating conditions</b>	<b>3</b>
<b>9</b>	<b>Static characteristics</b>	<b>4</b>
<b>10</b>	<b>Dynamic characteristics</b>	<b>5</b>
<b>11</b>	<b>Waveforms</b>	<b>6</b>
<b>12</b>	<b>Package outline</b>	<b>8</b>
<b>13</b>	<b>Abbreviations</b>	<b>13</b>
<b>14</b>	<b>Revision history</b>	<b>13</b>
<b>15</b>	<b>Legal information</b>	<b>14</b>
15.1	Data sheet status	14
15.2	Definitions	14
15.3	Disclaimers	14
15.4	Trademarks	14
<b>16</b>	<b>Contact information</b>	<b>14</b>
<b>17</b>	<b>Contents</b>	<b>15</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

founded by

**PHILIPS**

© NXP B.V. 2008.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 18 September 2008

Document identifier: 74HC\_HCT02\_3